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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/733,418	12/08/00	AKRAM	S 96-0841.01

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EXAMINER	
BROCK, J.	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/18/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

Office Action Summary	Application No.	Applicant(s)	
	09/733,418	AKRAM, SALMAN	
	Examin r	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the corr spond nce addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-56* is/are pending in the application.

4a) Of the above claim(s) *32,39,42,44-49 and 55* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-31,33-38,40,41,43,50-54 and 56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species I in Paper No. 5 is acknowledged.

After further review of the claims it has been determined that claim 44 clearly reads on non-elected Species II and therefore has not been examined further.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 25 recites the limitation "the semiconductive spacer" in eighth line of the claim. There is insufficient antecedent basis for this limitation in the claim. The limitation "the semiconductive spacer" will be treated as "the spacer".

4. Claims 26, 35, 41 and 51 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase "at least approximately 90%" renders the claim indefinite because it is unclear what the concentration of conductive ions that define the diffusion region actually is.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 50 – 54 and 56 are rejected under 35 U.S.C. 102(b) as being anticipated by Sasaki (USPAT 4471525).

With regard to claim 50, Sasaki discloses in figure 8a forming a trench (115) into a semiconductor substrate (111). Sasaki discloses in figure 8b forming a dielectric lining (116) on the surface of the trench. Sasaki discloses in figure 8c forming a semiconductive spacer (120) along the sidewall of the trench. Sasaki discloses in figure 8d forming an insulative material (122 and 123) in the trench, the insulative material substantially consuming the semiconductive spacer and thereby substantially filling the trench.

With regard to claim 51, Sasaki discloses in figure 8e wherein an overall depth of the trench is two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms.

With regard to claim 52, Sasaki discloses in figures 8a further comprising the step of forming an insulation layer (112) on the semiconductor substrate prior to the step of forming a first trench.

With regard to claim 53, Sasaki discloses in figures 8c and 8d annealing the semiconductor assembly in the presence of an oxidizing agent.

With regard to claim 54, Sasaki discloses in figure 8d, column 15, line 36 and column 17, line 15 wherein the insulative material and the dielectric lining are the same material.

With regard to claim 56, Sasaki discloses in figures 8a – 8d wherein the process uses only one mask (114) to form the device isolation.

7. Claims 25 – 29, 33, 50, 52 and 56 are rejected under 35 U.S.C. 102(e) as being anticipated by Akram (USPAT 5895253).

With regard to claim 25, Akram discloses in figure 8 forming a first trench (82) into a semiconductor substrate (64). Akram discloses in figure 9 forming a dielectric lining (92) on the surface of the first trench. Akram discloses in figure 10 forming a spacer (94) along the sidewall of the first trench. Akram discloses in figure 11 forming a second trench (112) into the semiconductor substrate assembly at the bottom of the first trench by using the spacer as an etching guide. Akram discloses in figure 12 forming an insulative material (122) in the first and second trenches, the insulative material substantially filling the first and second trenches.

With regard to claim 26, As far as the examiner can ascertain Akram reads on the claimed invention.

With regard to claim 27, Akram discloses in column 5, lines 6 and 7 wherein the spacer is formed from an oxidizable material.

With regard to claim 28, Akram discloses in column 5, lines 5 and 6 wherein the spacer is formed of oxide.

With regard to claim 29, Akram discloses in figures 7a and 7b further comprising the step of forming an insulation layer (62) on the semiconductor substrate prior to the step of forming a first trench.

With regard to claim 33, Akram discloses in figures 7a, 7b and 8 – 12 wherein the process uses only one mask (72) to form the device isolation.

With regard to claim 50, Akram discloses in figure 8 forming a trench (82) into a semiconductor substrate (64). Akram discloses in figure 9 forming a dielectric lining (92) on the surface of the trench. Akram discloses in figure 10 forming a semiconductive spacer (94) along the sidewall of the trench. Akram discloses in figure 12 forming an insulative material (122) in the trench, the insulative material substantially consuming the semiconductive spacer and thereby substantially filling the trench.

With regard to claim 52, Akram discloses in figures 7a and 7b further comprising the step of forming an insulation layer (62) on the semiconductor substrate prior to the step of forming a first trench.

With regard to claim 56, Akram discloses in figures 7a, 7b and 8 – 12 wherein the process uses only one mask (72) to form the device isolation.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 25 – 31, 33 – 38, 40, 41 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki in view of Kameyama (USPAT 4472240).

With regard to claim 25, Sasaki discloses in figure 8a forming a first trench (115) into a semiconductor substrate (111). Sasaki discloses in figure 8b forming a dielectric lining (116) on the surface of the first trench. Sasaki discloses in figure 8c forming a spacer (120) along the sidewall of the first trench. Sasaki discloses in figure 8c using the spacer as an etching guide to etch the dielectric lining. Sasaki discloses in figure 8d forming an insulative material (123 and 122) in the first trench, the insulative material substantially filling the first trench. Sasaki does not disclose forming a second trench into the semiconductor substrate assembly at the bottom of the first trench while using the spacer as an etching guide. Kameyama teaches in figure 4e forming a second trench (107) into the semiconductor substrate assembly at the bottom of a first trench (104) by using a spacer (106a and 106b) as an etching guide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the etching of the second trench of Kameyama in the method of Sasaki in order to form an element isolation region in a self-aligned manner with excellent controllability without forming a cavity therein as stated by Kameyama in column 2, lines 51 – 55. Kameyama also teaches in column 4, lines 18 – 25 forming an oxide filler in the first and second trenches substantially filling the first and second trenches. Therefore, it would further have been obvious to combine the method of filling the trenches of Sasaki and Kameyama.

With regard to claim 26, Sasaki discloses in figure 8e wherein an overall depth of the first trench is two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration

of conductive atoms. It would be further obvious in the method of Sasaki and Kameyama that the depth of the first and second trench would have been two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms.

With regard to claim 27, Sasaki discloses in figures 8c and 8d wherein the spacer is formed from an oxidizable material.

With regard to claim 28, Kameyama discloses in column 3, lines 60 – 68 wherein the spacer is formed of oxide.

With regard to claim 29, Sasaki discloses in figures 8a further comprising the step of forming an insulation layer (112) on the semiconductor substrate prior to the step of forming a first trench.

With regard to claim 30, Sasaki discloses in figures 8c and 8d annealing the semiconductor assembly in the presence of an oxidizing agent.

With regard to claim 31, Sasaki discloses in figure 8d, column 15, line 36 and column 17, line 15 wherein the insulative material and the dielectric lining are the same material.

With regard to claim 32, Sasaki discloses in figures 8c and 8d wherein the dielectric lining inhibits becoming oxidized.

With regard to claim 33, Sasaki discloses in figures 8a – 8d wherein the process uses only one mask (114) to form the device isolation.

With regard to claim 34, Sasaki discloses in figure 8a forming a first trench (115) into a semiconductor substrate (111). Sasaki discloses in figure 8b forming a dielectric lining (116) on the surface of the first trench. Sasaki discloses in figure 8c forming a semiconductive spacer

(120) along the sidewall of the first trench. Sasaki discloses in figure 8c using the semiconductive spacer as an etching guide to etch the dielectric lining. Sasaki discloses in figure 8d forming an insulative material (123 and 122) in the first trench, the insulative material substantially consuming the semiconductive spacer and thereby substantially filling the first trench. Sasaki does not disclose forming a second trench into the semiconductor substrate assembly at the bottom of the first trench while using the spacer as an etching guide. Kameyama teaches in figure 4e forming a second trench (107) into the semiconductor substrate assembly at the bottom of a first trench (104) by using a spacer (106a and 106b) as an etching guide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the etching of the second trench of Kameyama in the method of Sasaki in order to form an element isolation region in a self-aligned manner with excellent controllability without forming a cavity therein as stated by Kameyama in column 2, lines 51 – 55. Kameyama also teaches in column 4, lines 18 – 25 forming an oxide filler in the first and second trenches substantially filling the first and second trenches. Therefore, it would further have been obvious to combine the method of filling the trenches of Sasaki and Kameyama. Sasaki discloses in figures 8d – 9b planarizing the insulative material. Sasaki discloses in figure 8a wherein the process uses only one mask to form the device isolation.

With regard to claim 35, Sasaki discloses in figure 8e wherein an overall depth of the first trench is two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms. It would be further obvious in the method of Sasaki and Kameyama that the depth of the first and second trench would have been two times the depth of a bordering

diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms.

With regard to claim 36, Sasaki discloses in figures 8a further comprising the step of forming an insulation layer (112) on the semiconductor substrate prior to the step of forming a first trench.

With regard to claim 37, Sasaki discloses in figures 8c and 8d annealing the semiconductor assembly in the presence of an oxidizing agent.

With regard to claim 38, Sasaki discloses in figure 8d, column 15, line 36 and column 17, line 15 wherein the insulative material and the dielectric lining are the same material.

With regard to claim 40, Sasaki discloses in figure 8a forming a first mask (114) over a silicon substrate (111) assembly. Sasaki discloses in figure 8a forming a first trench (115) into the silicon substrate assembly using the mask as an etching guide. Sasaki discloses in figure 8b forming an oxide layer (116) on the surface of the first trench. Sasaki discloses in figure 8c forming a silicon spacer (120) on the sidewall of the first trench. Sasaki discloses in figure 8c using the silicon spacer as an etching guide to etch the dielectric lining. Sasaki discloses in figure 8d forming an oxide filler (123 and 122) in the first trench, the oxide filler substantially consuming the silicon spacer and thereby substantially filling the first trench. Sasaki does not disclose forming a second trench into the semiconductor substrate assembly at the bottom of the first trench while using the spacer as an etching guide. Kameyama teaches in figure 4e forming a second trench (107) into the semiconductor substrate assembly at the bottom of a first trench (104) by using a spacer (106a and 106b) as an etching guide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the etching of the second

trench of Kameyama in the method of Sasaki in order to form an element isolation region in a self-aligned manner with excellent controllability without forming a cavity therein as stated by Kameyama in column 2, lines 51 – 55. Kameyama also teaches in column 4, lines 18 – 25 forming an oxide filler in the first and second trenches substantially filling the first and second trenches. Therefore, it would further have been obvious to combine the method of filling the trenches of Sasaki and Kameyama. Sasaki discloses in figures 8d – 9b planarizing the oxide filler.

With regard to claim 41, Sasaki discloses in figure 8e wherein an overall depth of the first trench is two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms. It would be further obvious in the method of Sasaki and Kameyama that the depth of the first and second trench would have been two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms.

With regard to claim 43, Sasaki discloses in figures 8c and 8d annealing the semiconductor assembly in the presence of an oxidizing agent.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hsu et al., Liou et al., Ezaki, Ishiuchi, Wu, Sheng et al., Dennison et al., Lee and Mehta all disclose forming trench isolation using a sidewall as an etching mask.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
October 15, 2001

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